UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,397	04/28/2005	Jean Nicolai	859063.536USPC	4398

38106 7590 09/25/2007

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 5400
SEATTLE, WA 98104-7092

EXAMINER	
ABDELNOUR, AHMED F	

ART UNIT	PAPER NUMBER
2624	

MAIL DATE	DELIVERY MODE
09/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,397	NICOLAI ET AL.	
	Examiner	Art Unit	
	Farras Abdelnour	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *June 28, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6-9, and 12 rejected under 35 U.S.C. 102(b) as being anticipated by Fatemi *et al.* (Fatemi, O.; Panchanathan, S.P., "Fractal engine: an affine video processor core for multimedia applications," Circuits and Systems for Video Technology, IEEE Transactions on, vol.8, no.7, pp.892-908, Nov 1998).

Regarding Claim 1, Fatemi *et al.* teaches method for storing values of a range block and of seven isometries used in a fractal image compression method ("isometric transforms:

I_1 —identity;

I_2, I_3 —reflection about the midvertical line and the midhorizontal line;

I_4, I_5 —reflection about the first diagonal and the second diagonal;

I_6, I_7, I_8 —rotation around the center by 90, 180, and 270," page 897, column 2. Also see "Barnsely [8] has proposed an algorithm to compress fractal images with a very high compression ratio (100–10 000)," page 902, column 2), comprising using four memory areas of identical sizes in which are respectively stored an identity, and three first isometries corresponding to the isometries of symmetry with respect to a vertical axis, of 270° rotation, and of 90° rotation ("Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90).

Regarding Claim 6, Fatemi *et al.* teaches a method, comprising: obtaining a reference block of pixels from an image ("The image is partitioned into nonoverlapping blocks called range blocks," page 897, column 1);

performing transformation on the reference block to obtain a plurality of isometries corresponding to isometries of symmetry with respect to at least one axis and with respect to at least one rotation of the reference block ("Affine Transforms: A set of special affine transforms typically used in several image and video processing applications is applied on a square block of pixels ($L = M \times M$ pixels), resulting in transformations such as transposition, rotation, translation, and scaling," page 897, column 2); and

storing values representative of the reference block and values representative of the isometries ("Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90).

Regarding Claim 7, Fatemi *et al.* teaches the method of claim 6 wherein storing the values representative of the reference block and of the isometries includes storing these values in memory areas of identical sizes ("Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90).

Regarding Claim 8, Fatemi *et al.* teaches the method of claim 6 wherein performing transformation on the reference block to obtain the plurality of isometries includes obtaining the isometries of symmetry with respect to a vertical axis, a 270° rotation, and a 90° rotation ("isometric transforms:

I_1 —identity;

I_2, I_3 —reflection about the midvertical line and the midhorizontal line;

I_4, I_5 —reflection about the first diagonal and the second diagonal;

I_6, I_7, I_8 —rotation around the center by 90, 180, and 270," page 897, column 2).

Regarding Claim 9, Fatemi *et al.* teach the method of claim 8 wherein performing transformation on the reference block to obtain the plurality of isometries further

includes obtaining the isometries of symmetry with respect to a horizontal axis, a 180° rotation, a first diagonal, and a second diagonal rotation ("isometric transforms:

I_1 —identity;

I_2, I_3 —reflection about the midvertical line and the midhorizontal line;

I_4, I_5 —reflection about the first diagonal and the second diagonal;

I_6, I_7, I_8 —rotation around the center by 90, 180, and 270," page 897, column 2).

Regarding Claim 12, Fatemi *et al.* teaches the method The method of claim 1 wherein storing values representative of the isometries includes storing at least two of the isometries in a same memory area ("Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5, 10, 11, and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Fatemi *et al.* as applied to claim 1 above, and further in view of Tsukasa *et al.* US 6714451 B2 ("Semiconductor memory device including bit select circuit").

Regarding Claim 2, Fatemi *et al.* discloses storing isometries corresponding to identity, vertical and horizontal axes, 90°, 180°, 270°, first, and second diagonals. Fatemi *et al.* does not explicitly disclose further comprising reading from the memory areas, wherein each memory area is addressed in a first direction for a reading of the stored values to obtain the identity and the first three isometries, and in a reverse direction for a reading of the four other isometries of symmetry with respect to a horizontal axis, of 180° rotation, of symmetry with respect to a first diagonal, and of symmetry with respect to a second diagonal.

Tsukasa *et al.* teaches forward reading ("Transistor QN115 is connected between ground node 6 and transistor QN11 and a reverse write signal WRITE-R or a forward read signal READ-F is inputted into the gate of transistor QN115. Reverse write signal WRITE-R is a signal which is outputted from control circuit 17 when data is written to the second storage region of binary storage type nonvolatile memory cell WMC. Forward read signal READ-F is a signal which is outputted from control circuit 17 when data is read from the first storage region of binary storage type nonvolatile memory cell WMC," column 15, lines 1-10).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to apply Tsukasa's forward and backward reading circuits to Fatemi's fractal compression implementation to images and videos for the purpose of fast and efficient storage and retrieval of data.

Regarding Claim 3, the combination Fatemi-Tsukasa teaches fractal image compression method using a range block and seven isometries of this block (See Section III.B of Fatemi, page 897), the method comprising:
-memorizing respective values of the pixels of the range block and of only three of its isometries (See "Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90, both in Fatemi); and
-addressing corresponding memory areas in read mode in one direction or in a reverse direction according to a desired isometry (See Tsukasa, column 15, lines 1-10).

Regarding Claim 4, the combination Fatemi-Tsukasa teaches the method of claim 3; wherein two isometries of the range block are stored in a same memory area (See "Random Access Memory (RAM): This module stores input data, intermediate results, and output data," page 899, column 2. Also consult Fig. 13, page 90, both in Fatemi).

Regarding Claim 5, the combination Fatemi-Tsukasa teaches a circuit for addressing a memory of storage of an image data range block intended to be used in a fractal image compression method (Consult Fig. 13 in Fatemi, page 900), the circuit including means for addressing each of four areas of said memory in a first direction and in a reverse direction (See Tsukata, column 15, lines 1-10).

Regarding Claim 10, the combination Fatemi-Tsukasa teaches the method of claim 9, further comprising: reading a memory area, in a first direction, having stored therein the values representative of the reference block and values representative of the isometries of symmetry with respect to the vertical axis, the 270° rotation, and the 90° rotation (See Fig. 13 in Fatemi, and Tsukata, column 15, lines 1-10); and reading the memory area, in a second direction different from the first direction, having stored therein the values representative of the isometries of symmetry with respect to the horizontal axis, the 180° rotation, the first diagonal, and the second diagonal (See Fig. 13 in Fatemi, and Tsukata, column 15, lines 1-10).

Regarding Claim 11, the combination Fatemi-Tsukasa teaches the method of claim 10 wherein reading the memory area in the second direction includes reading the memory area in a reverse direction relative to the first direction (See Tsukata, column 15, lines 1-10).

Regarding Claim 13, the combination Fatemi-Tsukasa teaches the method of claim 1, further comprising reading particular ones of the memory area, having values stored therein, in a forward direction or in a reverse direction according to an isometry that is to be compared with a domain block of pixels of the image (See Fig. 13 in Fatemi, and Tsukata, column 15, lines 1-10).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Barnsley *et al.* US 5347600 A ("Method and apparatus for compression and decompression of digital image data"); Bhunia, S.K.; Ghosh, S.K.; Kumar, P.; Das, P.P.; Mukherjee, J., "Design, simulation and synthesis of an ASIC for fractal image coding," VLSI Design, 1999. Proceedings. Twelfth International Conference On, vol., no., pp.544-547, 7-10 Jan 1999. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Farras Abdelnour whose telephone number is 571-270-1806. The examiner can normally be reached on Mon. - Thurs. 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian P. Werner can be reached on 571-272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Farras Abdelnour
Examiner
Art Unit 2624

FA

WENPENG CHEN
PRIMARY EXAMINER

9/19/07